Amendments to the Specification:

Please replace paragraph 0029, 0044 with the following replacement paragraphs:

0029 A memory controller 31 communicates with non-volatile memory 14 to form a bulk memory storage 26. Thus, bulk storage memory 26 can be constructed of a memory controller 12, connected to the computer system bus 20, and an array of non-volatile memory integrated circuit chips. Data and instructions can be communicated from memory controller 12 to such an array over a serial data line 18. Similarly, data and status signals may be communicated from non-volatile memory 14 to memory controller 12 over serial data lines 16. In one embodiment, each one of the serial data lines 16 and 18 is a multi-bit (e.g., 16-bit) serial bus having I/O terminals 8 for electrical coupling. Other control and status circuits between memory controller 12 and non-volatile memory 14 are not shown in FIG. 1. Those skilled in the art can appreciate that the system depicted in FIGS. 1 to 4 is presented for illustrative purposes only.

0044 Traditionally, each spare column is reserved for repairing one column corresponding to a specific I/O terminal. If there are 16 I/O terminals (e.g., I/O terminals 8 described with reference to FIG.'s 1-4) for a 16-bit data bus (e.g., multi-bit serial data lines 16 and 18 described with reference to FIG.'s 1-4), then 16 spare columns would normally be required to support a one-time repair of any possible column out of the 16 columns accessed at one time. To improve repairing efficiency, the columns for two or more I/O terminals can be made to share a single spare column, in a more complicated design. In the specific embodiment described above, all columns associated with a set of four I/O terminals share a single set of five spare columns. The (16,11) Hamming code is well known in the art and is described at pg. 64 of "Error Control Coding: Fundamentals and Applications," by Shu Lin & Daniel J. Costello, Jr.).